AF 2111

PATENT APPLICATION
Attorney's Do. No. 5087-27

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	David H. Harris, Gordon R. Clark and Stephen D. Holland		
Serial No.	09/990,739	Examiner:	Dang, Khanh
Confirmation No.:	3310		
Filed:	November 16, 2001	Group Art Unit:	2111
For:	UNIVERSAL SERIAL BUS (USB) INTERFACE FOR MASS STORAGE DEVICE		

TRANSMITTAL LETTER

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Enclosed for filing in the above-referenced application are the following:

- ☒ Appellant's Brief (in Support of Appeal), in triplicate
- ☒ Exhibits 1, 2 and 3
- ☒ Filing Fee
- ☒ PTO Form 2038 authorizing credit card payment in the amount of $500.00 for the above-listed fee
- ☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703. A duplicate copy of this sheet is enclosed.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Craig R. Rogers, Reg. No. 43,888

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613

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Date: April 18, 2005

Deanna Brusco

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APPELLANT'S BRIEF

UNDER 37 CFR §1.192

Appeal is taken from the Examiner's Office Action mailed February 2, 2005, finally rejecting claims 1-20 in the instant application.

This Appeal Brief is in furtherance of the Notice of Appeal mailed in this case on March 2, 2005.

The fees required under §1.17(c) and any required petition for extension of time for filing this Brief and fees therefor are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This Brief is transmitted in triplicate.

This Brief contains these items under the following headings, and in the order set forth below.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST
37 CFR §1.192(c) (1)

Cypress Semiconductor Corp. is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES
37 CFR §1.192(c) (2)

There are no other appeals or interferences known to Appellant, the Appellant's representative, or assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS
37 CFR §1.192(c) (3)

Status of All the Claims:

1. Claims presented: 1-20
2. Claims withdrawn from consideration but not cancelled: NONE
3. Claims cancelled: NONE
4. Claims pending: 1-20, of which,
   a. Claims allowed: NONE
   b. Claims objected to: NONE
   c. Claims rejected: 1-20

All of the rejected claims, namely claims 1-20, are being appealed. The appealed claims are eligible for appeal, having been finally rejected.

IV. STATUS OF AMENDMENTS
37 CFR § 1.192(c)(4)

On April 7, 2004, the Examiner issued an Office Action rejecting original claims 1-20 under 35 U.S.C. § 102(e) as being anticipated by Jacobs. The Examiner further identified supposed defects in a 37 CFR 1.131 declaration and redacted exhibit, which were submitted by one of the named inventors on January 9, 2003 to swear behind a reference identified by Applicant in an Information Disclosure Statement.

On August 9, 2004, Applicant responded to the April 7, 2004 Office Action by filing a new declaration by each of the inventors under 37 C.F.R. 1.131, along with an unredacted Exhibit, swearing behind the Jacobs reference. On October 28, 2004, the Examiner issued a Final Office Action repeating the rejections under Jacobs and rejecting Applicants 37 CFR 1.131 declarations and arguments related thereto.

On December 16, 2004, Applicant responded by identifying the Examiner's failure to adequately consider the earlier submitted 37 CFR 1.131 declarations. On February 19, 2004, the Examiner issued an Advisory Action again rejecting claims 1-20 stating that Applicant's response did "NOT place the application in condition for allowance because: Applicant's Affidavit filed on August 16, 2004 fails to overcome the prior art because of the reasons set forth in the Final Rejection." On March 2, 2005, Applicant responded by filing a Notice of Appeal.

V. SUMMARY OF THE INVENTION
37 CFR §1.192(c) (5)

The invention disclosed and claimed in the present application relates generally to a bridging circuit for translating ATA/ATAPI signals from a mass storage device into USB signals. The USB signals can, for instance, be provided to a host computer through a USB port. In a preferred embodiment, the bridging circuit is provided in a single bridging chip. The bridging circuit can be located on a motherboard of the mass storage device or a secondary board. Methods relating to the use of a bridging circuit are also disclosed and claimed.

VI. ISSUES ON APPEAL
37 CFR §1.192(c) (6)

The Examiner rejected claims 1-20 under 35 U.S.C. § 102(e) as being anticipated by Jacobs. No other references were cited as a basis for rejecting Applicant's claims. For the convenience of the Board of Appeals, the entire Final Office Action dated October 28, 2004 and the Advisory Action dated February 2, 2005 have been reproduced and attached as Exhibits 1 and 2, respectively. Applicant's Amendment After Final Rejection, dated December 16, 2004 is also attached hereto for the convenience of the Board of Appeals as Exhibit 3.

The issue before the Board of Appeals is:

A. Whether the Examiner improperly ignored Applicant's 37 CFR 1.131 declarations

submitted August 9, 2004.

VII. GROUPING OF CLAIMS
37 CFR §1.192(c) (7)

A. The Jacobs Reference

The Examiner rejected claims 1-20 under 35 U.S.C. § 102(e) as being anticipated by Jacobs (U.S. Patent No. 6,618,788). The Examiner further rejected Applicant's arguments, which asserted that Jacobs was not appropriately considered as prior art because Applicant's date of invention was prior to the September 27, 2000 filing date of Jacobs. Specifically, the Examiner stated:

> Applicant's 37 CFR 1.131 Affidavit filed 8/16/2004 have been fully considered but it fails to overcome the prior art because of the following reasons.
>
> 1) The Declaration alleged that "a universal serial bus (USB) interface for mass storage device as described and claimed in the application" was conceived and developed before October 5, 2000. However, the declaration does not include facts showing a completion of the invention prior to October 5, 2000. The Exhibit "A" shows only a Product Data Sheet of bridge chip (ISD-300 ASIC). Further, there's no indication/evidence from the document showing Applicant's involvement with the product. Still further, there is no specific date on the document. As a matter of fact, a close examination of the ISD-300 ASIC Product Data Sheet (Revision 0.8), page 5, submitted by the Applicant, reveals that the actual dates ("Copyright" date and ["]Document Revision History") of this document have been intentionally made blank. However, a copy of ISD-300 ASIC Product Data Sheet available to this Office clearly shows January 16, 2001 is the "Creation Time/Date" of Revision 0.8.
>
> 2) The prior art is claiming the same invention.

VIII. ARGUMENT
37 CFR § 1.192(c) (8)

The Examiner improperly ignored Applicant's 37 CFR 1.131 declarations submitted on August 9, 2004 from each of the inventors. Although the Examiner appears to reference

Applicant's August submission,[1] the Examiner appears only to have considered the affidavit and evidence filed January 9, 2003 and not the affidavits and evidence submitted on August 9, 2004.

For example, the Examiner states that the "[d]eclaration alleged that 'a universal serial bus (USB) interface for mass storage device as described and claimed in the application' was conceived and developed before October 5, 2000." (Final Office Action, p. 7). However, the August 9, 2004 declarations each state that the named inventors conceived of and developed the claimed invention before "September 27, 2000." The submitted declarations further establish both completion of the invention prior to September 27, 2000 and Applicants' involvement with that invention, specifically stating that the "[b]efore September 27, 2000, [the] named inventors ... conceived of and developed a universal serial bus (USB) interface for mass storage device as described and claimed in the application." The declarations further explain that the "the ISD300 chip," described in detail in the attached datasheet "created before September 27, 2000," is "identified in the application as one of the preferred embodiments of the invention."

The Examiner also incorrectly states that "there is no specific date on the document" and that "a close examination of the ISD-300 ASIC Product Data Sheet (Revision 0.8), page 5, submitted by the Applicant, reveals that the actual dates ('Copyright' date and Document Revision History') of this document have been intentionally made blank." (Final Office Action, p. 7). These dates were clearly provided in the exhibit accompanying the August 9, 2004 declarations to assuage the Examiner's previously expressed concerns.

In addition, the Examiner never provided Applicant with a copy of the data sheet that was represented as being "available to [that] Office" to allow Applicant to fully address the Examiner's arguments. In any event, the evidence submitted with the August 9, 2004

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[1] Although the Examiner identifies "Applicant's 37 CFR 1.131 affidavit filed 8/16/2004," there was no submission made on that date. Although it is possible the Examiner is referring to the August 9, 2004 submissions, there were actually three separate 37 CFR 1.131 declarations filed on that date, and it does not appear that the Examiner considered either the substance of those declarations or the Exhibit that accompanied those declarations.

declarations clearly shows the "Creation Date/Time" of the initial revision (0.1) as May 11, 2000, with this particular Revision (0.8) being dated September 4, 2000.

Finally, it should be noted that Jacobs does not claim the same invention as recited in the claims of the present application. Although there is some overlapping subject matter in the applications, the claims of the present application do not appear to be coextensive in scope and subject matter with the claims in Jacobs.

IX. CONCLUSION

For the foregoing reasons, Appellant requests that the Board reverse the Examiner's rejections to Appellant's claims.

Respectfully submitted,

MARGER JOHNSON & MCCOLLOM, P.C.

Craig R. Rogers
Registration No. 43,888

MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, Oregon 97205
(503) 222-3613

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Date: April 18, 2005

Deanna Brusco

X. APPENDIX
37 CFR § 1.192(c) (9)

The text of the claims on appeal (1-20) is:

1. A method of communicating with a mass storage device, comprising:

receiving ATA/ATAPI signals from a mass storage device into a bridging circuit;

converting the ATA/ATAPI signals from the mass storage device into USB signals using the bridging circuit; and

outputting the USB signals from the bridging circuit.

2. A method according to claim 1, wherein the bridging circuit is provided in a single, bridging chip.

3. A method according to claim 1, wherein the bridging circuit is provided on a motherboard of the mass storage device.

4. A method according to claim 1, wherein the bridging circuit is provided on a secondary board.

5. A method according to claim 4, wherein a mass storage device motherboard outputs ATA/ATAPI signals, and wherein the secondary board receives the ATA/ATAPI signals from the mass storage device motherboard and converts them into USB signals.

6. A motherboard for a mass storage device, said motherboard comprising:

input logic configured to receive an input signal from a read unit of the mass storage device;

a bridging circuit configured to receive the input signal from the input logic and convert the input signal into a USB signal; and

output circuitry configured to output the USB signal from the motherboard.

7. A mass storage device motherboard according to claim 6, wherein the bridging circuit comprises a bridging chip for converting the input signal into the USB signal.

8. A mass storage device motherboard according to claim 6, wherein the bridging chip comprises:

an ATA/ATAPI interface configured to receive ATA/ATAPI signals from the input logic;

a disk interface configured to receive ATA/ATAPI signals from the ATA/ATAPI interface;

a serial interface engine; and

a USB physical interface transceiver configured to receive signals from the serial interface engine and output USB signals to a USB interface.

9. A secondary board configured to enable communication between a mass storage device motherboard and a host motherboard, said secondary board comprising:

a connector port for receiving signals from the mass storage device motherboard;

a bridging circuit for converting signals from the mass storage device motherboard into USB signals; and

a USB connector port for outputting the USB signals to the host motherboard.

10. A secondary board according to claim 9, wherein the bridging circuit comprises a bridging chip configured to translate the signals from the mass storage device motherboard into USB signals.

11. A secondary board according to claim 10, wherein the bridging chip comprises a USB physical interface transceiver, a serial interface engine, and a disk interface.

12. A secondary board according to claim 11, wherein the disk interface receives

ATA/ATAPI signals through an ATA/ATAPI interface, and wherein the ATA/ATAPI signals are converted into USB 2.0 signals and are output to a USB Interface through the USB physical interface transceiver.

13. A bridging chip comprising:
an input configured to receive ATA/ATAPI signals;
conversion logic configured to convert the ATA/ATAPI signals into USB signals; and
an output configured to output the USB signals.

14. A chip according to claim 13, wherein said input comprises an ATA/ATAPI interface arranged to receive the ATA/ATAPI signals and a disk interface configured to receive ATA/ATAPI signals from the ATA/ATAPI interface; wherein said conversion logic comprises a serial interface engine and a USB physical interface transceiver, said interface transceiver being configured to receive signals from the serial interface engine and output USB signals to a USB interface.

15. A chip according to claim 13, wherein the chip is located on a mass storage device motherboard.

16. A chip according to claim 13, wherein the chip is located on a secondary board.

17. A chip according to claim 16, wherein the secondary board is arranged to receive ATA/ATAPI signals from a motherboard of the mass storage device.

18. A method of converting signals from a mass storage device into USB signals, said method comprising:
receiving a signal from a mass storage device into a bridging chip;
converting the signal from the mass storage device into a USB signal;
outputting the USB signal from the bridging chip.

19. A method of converting signals according to claim 18, wherein said bridging chip is located on a motherboard of the mass storage device.

20. A method of converting signals according to claim 18, wherein the bridging chip is located on a secondary board arranged in communication with a motherboard of the mass storage device.

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Date: April 18, 2005

Deanna Brusco

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,739	11/16/2001	David H. Harris	5087-27	3310

20575 7590 10/28/2004

MARGER JOHNSON & MCCOLLOM PC
1030 SW MORRISON STREET
PORTLAND, OR 97205

EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 10/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

EXH 1
PAGE 1 OF 9

Office Action Summary	Application No.	Applicant(s)	
	09/990,739	HARRIS ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

EXH 1

PAGE 2 OF 9

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Jacobs.

At the outset, it is noted that similar claims will be grouped together to avoid repetition.

As broadly drafted, these claims do not define any structure/step that differs from Jacobs.

With regard to claim 1, Jacobs discloses a method of communicating with a mass storage device, comprising: receiving ATA/ATAPI signals from a mass storage device (140) into a bridging circuit (156); converting the ATA/ATAPI signals from the mass storage device (140) into USB signals using the bridging circuit (156); and outputting the USB signals from the bridging circuit (156).

With regard to claim 2, in Jacobs, the bridging circuit (156) can be provided in a single IC.

With regard to claim 3, the bridging circuit (156) is provided on a motherboard of the mass storage device (see Fig. 6 and description thereof).

With regard to claim 4, the bridging circuit (156) is provided on a secondary board (physical device 160, see Figs. 7 and 8, and description thereof).

With regard to claim 5, the mass storage device (186) motherboard outputs ATA/ATAPI signals, and wherein the secondary board (of physical device 160) receives the ATA/ATAPI signals from the mass storage device (186) motherboard and converts them into USB signals (to host 130).

With regard to claim 6, Jacobs discloses a motherboard for a mass storage device (160), said motherboard comprising: input logic (ATA logic) configured to receive an input signal from a read unit of the mass storage device (160); a bridging circuit (156, Fig. 6) configured to receive the input signal from the input logic and convert the input signal into a USB signal; and output circuitry configured to output the USB signal from the motherboard (of the ATA device 160).

With regard to claim 7, the bridging circuit (156) comprises a bridging chip (IC) for converting the input signal into the USB signal.

With regard to claim 8, the bridging chip (156) comprises: an ATA/ATAPI interface (ATA interface interfacing ATA device) configured to receive ATA/ATAPI signals from the input logic; a disk interface (of ATA disk interface) configured to receive ATA/ATAPI signals from the ATA/ATAPI interface; a serial interface engine (USB interface interfacing the host 130); and a USB physical interface transceiver (USB

protocol requires USB physical interface transceiver to be in full compliance with USB specification) configured to receive signals from the serial interface engine and output USB signals to a USB interface (of host 130).

With regard to claim 9, Jacobs discloses a secondary board (of physical device 160) configured to enable communication between a mass storage device (186) motherboard and a host motherboard (of host 130), said secondary board comprising: a connector port (it is clear that connecting port is used to connect the secondary board to ATA device 186) for receiving signals from the mass storage device (186) motherboard; a bridging circuit (156) for converting signals from the mass storage device (186) motherboard into USB signals; and a USB connector port (USB port for connecting 160 to host 130) for outputting the USB signals to the host (130) motherboard. See also Figs. 7 and 8 and description thereof.

With regard to claim 10, the bridging circuit (156) comprises a bridging chip (IC) configured to translate the signals from the mass storage device motherboard into USB signals.

With regard to claim 11, the bridging chip (IC 156) comprises a USB physical interface transceiver (USB protocol requires USB physical interface transceiver to be in full compliance with USB specification), a serial interface
engine (USB interface), and a disk interface (ATA disk interface).

With regard to claim 12, the disk interface receives ATA/ATAPI signals through an ATA/ATAPI interface, and wherein the ATA/ATAPI signals are converted into USB

2.0 signals (USB 2.0 is also employed in Jacobs) and are output to a USB Interface through the USB physical interface transceiver.

With regard to claim 13, Jacobs discloses a bridging chip (IC 156) comprising: an input configured to receive ATA/ATAPI signals; conversion logic configured to convert the ATA/ATAPI signals into USB signals; and an output configured to output the USB signals. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 14, the input comprises an ATA/ATAPI interface arranged to receive the ATA/ATAPI signals and a disk interface configured to receive ATA/ATAPI signals from the ATA/ATAPI interface; wherein said conversion logic comprises a serial interface engine and a USB physical interface transceiver, said interface transceiver being configured to receive signals from the serial interface engine and output USB signals to a USB interface. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 15, the chip is located on a mass storage device motherboard. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 16, the chip is located on a secondary board. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 17, the secondary board is arranged to receive ATA/ATAPI signals from a motherboard of the mass storage device. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 18, Jacobs discloses a method of converting signals from a mass storage device into USB signals, said method comprising: receiving a signal from a mass storage device into a bridging chip; converting the signal from the mass storage device into a USB signal; outputting the USB signal from the bridging chip. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 19, the bridging chip is located on a motherboard of the mass storage device. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

With regard to claim 20, the bridging chip is located on a secondary board arranged in communication with a motherboard of the mass storage device. See explanation regarding to claims 1-12 above. See specifically Figs. 5-8, and description thereof.

Response to Arguments

Applicants' 37 CFR 1.131 affidavit filed 8/16/2004 have been fully considered but it fails to overcome the prior art because of the following reasons:

1) The Declaration alleged that "a universal serial bus (USB) interface for mass storage device as described and claimed in the application" was conceived and developed before October 5, 2000. However, the declaration does not include facts showing a completion of the invention prior to October 5, 2000. The exhibit "A" shows only a Product Data Sheet of bridge chip (ISD-300 ASIC). Further, there's no indication/evidence from the document showing Applicant's involvement with the product. Still further, there is no specific date on the document. As a matter of fact, a close examination of the ISD-300 ASIC Product Data Sheet (Revision 0.8), page 5, submitted by the Applicant, reveals that the actual dates ("Copyright" date and Document Revision History") of this document have been intentionally made blank. However, a copy of ISD-300 ASIC Product Data Sheet available to this Office clearly shows January 16, 2001 is the "Creation Time/Date" of Revision 0.8.

2) The prior art is claiming the same invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner

EXH 1
PAGE 9 OF 9

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,739	11/14/2001	David H. Harris	5087-27	3310

20575 7590 02/02/2005

MARGER JOHNSON & MCCOLLOM, P.C.
1030 SW MORRISON STREET
PORTLAND, OR 97205

EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 02/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EXH 2
PAGE 1 OF 3

Advisory Action	Application No.	Applicant(s)	
	09/990,739	HARRIS ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 20 December 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1-20*.

   Claim(s) withdrawn from consideration: _____.

EXH 2
PAGE 2 OF 3

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

Khanh Dang
Primary Examiner

Continuation of 5. does NOT place the application in condition for allowance because: Applicants' 37 CFR 1.131 affidavit filed 8/16/2004 fails to overcome the prior art because of the reasons set forth in the Final Rejection. Any newly presented argument will be fully responded in due course..

PATENT APPLICATION
Do. No. 5087-27

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	David H. Harris, Gordon R. Clark and Stephen D. Holland		
Confirmation No.:	3310		
Serial No.	09/990,739	Examiner:	Dang, Khanh
Filed:	November 16, 2001	Group Art Unit:	2111
For:	UNIVERSAL SERIAL BUS (USB) INTERFACE FOR MASS STORAGE DEVICE		

Date: December 16, 2004

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Responsive to the Office Action dated October 28, 2004, enclosed is an amendment in the above-identified application.

The fee has been calculated as shown below.

CLAIMS AS AMENDED					
For:	Number After Amendment	Previous Number	Extra	Rate	Additional Fee
Total Claims	20	-20*	0	x $50 =	$0
Independent Claims	5	-5**	0	x $200 =	$0
Extension of Time – 1st					$0
Extension of Time – 2nd					$0
Extension of Time – 3rd					$0
First Presentation of Multiple Dependent Claims					$0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					$0

*greater of twenty (20) or number for which fee has been paid
**greater of three (3) or number for which fee has been paid

☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Craig D. Rogers

Craig R. Rogers, Reg. No. 43,888

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

EXH 3
PAGE 1 OF 7

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:

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FOR TRADEMARKS 2900 CRYSTAL DRIVE ARLINGTON, VA 22202-3513

ON: December 16, 2004
Dawnee Pruett

PATENT APPLICATION
Docket No. 5087-27

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: David H. Harris, et al.

Serial No. 09/990,739 Examiner: Dang, Khanh

Confirmation No. 3310

Filed: November 16, 2001 Group Art Unit: 2111

For: UNIVERSAL SERIAL BUS (USB) INTERFACE FOR MASS STORAGE DEVICE

Date:

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

This document is responsive to the Office Action dated October 28, 2004.

The claims, as presently pending, are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

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PAGE 2 OF 7

IN THE CLAIMS

1. (Original) A method of communicating with a mass storage device, comprising:

receiving ATA/ATAPI signals from a mass storage device into a bridging circuit;

converting the ATA/ATAPI signals from the mass storage device into USB signals using the bridging circuit; and

outputting the USB signals from the bridging circuit.

2. (Original) A method according to claim 1, wherein the bridging circuit is provided in a single, bridging chip.

3. (Original) A method according to claim 1, wherein the bridging circuit is provided on a motherboard of the mass storage device.

4. (Original) A method according to claim 1, wherein the bridging circuit is provided on a secondary board.

5. (Original) A method according to claim 4, wherein a mass storage device motherboard outputs ATA/ATAPI signals, and wherein the secondary board receives the ATA/ATAPI signals from the mass storage device motherboard and converts them into USB signals.

6. (Original) A motherboard for a mass storage device, said motherboard comprising:

input logic configured to receive an input signal from a read unit of the mass storage device;

a bridging circuit configured to receive the input signal from the input logic and convert the input signal into a USB signal; and

output circuitry configured to output the USB signal from the motherboard.

EXH 3

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7. (Original) A mass storage device motherboard according to claim 6, wherein the bridging circuit comprises a bridging chip for converting the input signal into the USB signal.

8. (Original) A mass storage device motherboard according to claim 6, wherein the bridging chip comprises:

an ATA/ATAPI interface configured to receive ATA/ATAPI signals from the input logic;

a disk interface configured to receive ATA/ATAPI signals from the ATA/ATAPI interface;

a serial interface engine; and

a USB physical interface transceiver configured to receive signals from the serial interface engine and output USB signals to a USB interface.

9. (Original) A secondary board configured to enable communication between a mass storage device motherboard and a host motherboard, said secondary board comprising:

a connector port for receiving signals from the mass storage device motherboard;

a bridging circuit for converting signals from the mass storage device motherboard into USB signals; and

a USB connector port for outputting the USB signals to the host motherboard.

10. (Original) A secondary board according to claim 9, wherein the bridging circuit comprises a bridging chip configured to translate the signals from the mass storage device motherboard into USB signals.

11. (Original) A secondary board according to claim 10, wherein the bridging chip comprises a USB physical interface transceiver, a serial interface engine, and a disk interface.

12. (Original) A secondary board according to claim 11, wherein the disk interface receives ATA/ATAPI signals through an ATA/ATAPI interface, and wherein the ATA/ATAPI signals are converted into USB 2.0 signals and are output to a USB Interface through the USB physical interface transceiver.

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13. (Original) A bridging chip comprising:

an input configured to receive ATA/ATAPI signals;

conversion logic configured to convert the ATA/ATAPI signals into USB signals; and

an output configured to output the USB signals.

14. (Original) A chip according to claim 13, wherein said input comprises an ATA/ATAPI interface arranged to receive the ATA/ATAPI signals and a disk interface configured to receive ATA/ATAPI signals from the ATA/ATAPI interface; wherein said conversion logic comprises a serial interface engine and a USB physical interface transceiver, said interface transceiver being configured to receive signals from the serial interface engine and output USB signals to a USB interface.

15. (Original) A chip according to claim 13, wherein the chip is located on a mass storage device motherboard.

16. (Original) A chip according to claim 13, wherein the chip is located on a secondary board.

17. (Original) A chip according to claim 16, wherein the secondary board is arranged to receive ATA/ATAPI signals from a motherboard of the mass storage device.

18. (Original) A method of converting signals from a mass storage device into USB signals, said method comprising:

receiving a signal from a mass storage device into a bridging chip;

converting the signal from the mass storage device into a USB signal;

outputting the USB signal from the bridging chip.

19. (Original) A method of converting signals according to claim 18, wherein said bridging chip is located on a motherboard of the mass storage device.

20. (Original) A method of converting signals according to claim 18, wherein the bridging chip is located on a secondary board arranged in communication with a motherboard of the mass storage device.

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REMARKS

Claims 1-20 are pending. Claims 1-20 stand rejected under 35 U.S.C. 102(e) as being anticipated by Jacobs. On August 9, 2004, Applicant submitted 37 CFR 1.131 affidavits from each of the inventors to overcome Jacobs. Although the Examiner references "Applicant's 37 CFR 1.131 affidavit filed 8/16/2004," the Examiner appears only to have considered the affidavit and evidence filed January 8, 2003 and not the affidavits and evidence submitted on August 9, 2004.

The Examiner states that the "Declaration alleged that 'a universal serial bus (USB) interface for mass storage device as described and claimed in the application' was conceived and developed before October 5, 2000." (Final Office Action, p. 7). The August 9, 2004 declarations state that the named inventors conceived of and developed the claimed invention before "September 27, 2000." The submitted declarations establish both completion of the invention prior to September 27, 2000 and Applicants' involvement with that invention, specifically stating that the ISD-300 chip is disclosed as a preferred embodiment of their invention.

The Examiner also states that "there is no specific date on the document" and that "a close examination of the ISD-300 ASIC Product Data Sheet (Revision 0.8), page 5, submitted by the Applicant, reveals that the actual dates ('Copyright' date and Document Revision History') of this document have been intentionally made blank." (Final Office Action, p. 7). This is also incorrect. These dates, although redacted from the earlier submission, were provided along with the August 9, 2004 declarations to assuage the Examiner's previously expressed concerns. The Examiner has not provided Applicant with a copy of the data sheet that is represented by the Examiner as being "available to [that] Office." Applicant notes, however, that the evidence submitted with the August 9, 2004 declarations shows the "Creation Date/Time" of the initial revision (0.1) as May 11, 2000, with this Revision (0.8) being dated September 4, 2000.

Finally, Applicant notes that Jacobs does not claim the same invention as recited in the claims of the present application. While Applicant acknowledges overlapping subject matter of the disclosures, the claims of the present application do not appear to be coextensive in scope and subject matter with the claims in Jacobs.

For the foregoing reasons, reconsideration and allowance of claims 1-20 of the application is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

EXH 3

PAGE 6 OF 7

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Craig R. Rogers, Reg. No. 43,888

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613
Customer No. 20575

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ON: December 16, 2004
Deanna Brisco

EXH 3
PAGE 7 OF 7